HYSTERESIS-LIKE FLATBAND VOLTAGE INSTABILITIES IN Al/Ta$_2$O$_5$-SiO$_2$/Si STRUCTURES AND THEIR CONNECTION WITH *J-V* CHARACTERISTICS

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Flatband and current-voltage instabilities in unstressed Al/Ta$_2$O$_5$-SiO$_2$/Si structures were studied in details. It has been found that, after an initial run left on fresh samples, both *C-V* and *J-V* characteristics exhibit repeatable patterns. Precisely repeatable counterclockwise hysteresis-like loop in *C-V* characteristics occurs, while no significant hysteretic behaviour is observed in static *J-V* characteristics. The reduced instability in *J-V* characteristics is explained by mutual compensation of two opposite effects owing to the presence of trapped positive charges on slow traps in the interfacial SiO$_2$-like layer: (i) flatband voltage shift and (ii) lowering of Fowler-Nordheim tunnelling barrier for holes injected from the Si substrate. Correct determination of equivalent oxide thickness and fast interface state densities requires using the *C-V* curves obtained during the runs right, because progressive trapping on slow states occurs during the runs left. Value of the oxide charge is to be determined using the value of the flatband voltage obtained from the run left (after an initial run right), since it corresponds to the state of empty slow traps.

Key words: *C-V* hystersis; nanosized dielectric films; interface silicon/silicon dioxide

INTRODUCTION

High permittivity (high-*k*) dielectrics attracted important research interest in view of their application as replacements for silicon dioxide films in nanoscale devices [1]. An important issue related to the quality of high-*k* dielectrics is the presence of threshold and flatband voltage instability when sweeping the gate bias from negative to positive voltages and then back [2–11]. The nature of these instabilities is still matter of debate. Instabilities can be related to transition currents [12, 13], dielectric relaxation current [14, 15], dipole formation at the high-k/SiO$_2$ interface [16], Maxwell-Wagner instability in bilayer dielectric stacks [17] and trapping of electrons or holes on various types of traps [18, 19]. Although some attempts were made to explain all these phenomena with a unified model, as due to the bilayer structure itself of the high-*k* dielectrics [20], it appears that the mechanisms affecting the instabilities depend on the specific high-*k* dielectric

composition and fabrication conditions. In this paper we study the issue of flatband voltage instability in the case of Ta$_2$O$_5$. The above material was chosen since it is a high-*k* dielectric particularly appropriate for capacitors of dynamic random-access memories (DRAM) [21, 22]. Ta$_2$O$_5$ is also used as gate insulator in organic thin-film transistors [11]. The method of characterization used in this study is based on hysteresis in *C-V* characteristics of metal-insulator-Silicon structures containing the considered dielectric. Much earlier, an exhaustive study on capacitance-voltage properties of Ta$_2$O$_5$ based layers as thick as 70 nm was done by Oehrlein [23], by whom three hysteretic patterns were observed and attributed either to hole capture (or electron emission) or to electron capture. The clockwise hysteresis observed in [24] was attributed to the charging of the Ta$_2$O$_5$/SiO$_2$ interface in a metal-Ta$_2$O$_5$/SiO$_2$-Si structure. Specifically, 62 nm thick Ta$_2$O$_5$ layer over an unintentionally grown 4 nm thick SiO$_2$ interfacial layer was experimentally studied. Theoretical model explains

very well the obtained experimental results. Charging of the Ta_2O_5/SiO_2 interface is explained to occur by electron current flowing from the metal gate through a leaky Ta_2O_5 layer. Particularly important improvements of tantalum oxide insulating layer properties have been achieved since then [25], and hence the results obtained earlier could not be applied to nowadays structures. Therefore, only the films obtained by optimized processes deserve further attention and the instabilities observed in them have to be studied. The usual assumption that the general conclusions obtained on much thicker high-*k* or SiO_2 films can be used for thinner films is to be exploited with due consideration. Having that much thinner films are nowadays required, in this work we study films as thin as 10 nm containing an SiO_2-like interfacial layer as thin as 2 nm or thinner. In such thin interfacial layers tunnelling occurs even at voltages as high as 1 V, and hence the structures studied here will manifest substantially different behaviour in the low voltage range, up to approximately 3 V. In addition, we intend to clearly distinguish between the degradation and charge trapping effects, based on results of our previous works where a comprehensive leakage current model was developed [26, 27] and origin of stress-induced leakage currents [28] was identified. Under some circumstances, instability in *J-V* characteristics has also been observed [2]. It is not clear whether these two types of the instability have similar or different nature and behaviour. In this work we also aim to study simultaneously *J-V* and *C-V* instabilities, as well as the connection between them, in order to establish whether the mechanisms leading to these two instabilities are similar or different. In order to avoid bulk trapping and trap creation in the bulk of the insulating film at high fields, only voltages of absolute value up to 3 V were applied. For the considered dielectric with comparable thicknesses no significant bulk trapping effects were observed while studying stress induced traps in Al/Ta_2O_5-SiO_2/Si structures [29]. In addition, no significant current instability was observed for comparable fields on Ta_2O_5 layer in the time scale up to 10^3 s, when studying current instabilities on metal-Ta_2O_5-metal structures [30]. It is thus expected the effects observed sweeping the voltage between positive and negative values to be dominated by trapping on existing interfacial traps and charging/discharging of the interfaces. Under these conditions the alterations of *J-V* and *C-V* characteristics from one sweep to the next are expected to be small enough, thus allowing studying the instabilities as manifested predominantly by repeatable patterns.

EXPERIMENT

Chemically cleaned p-type (100) 15 Ωcm Si was used as substrate. After cleaning a Ta film was deposited on Si by sputtering of Ta target in Ar atmosphere. Subsequently, the Ta film was oxidized in dry O_2 at 550°C. More details on the sample preparation can be found in reference [21]. The oxidation temperature was chosen to be low enough to minimize the substrate oxidation and to prevent the formation of tantalum silicides. The thickness of the Ta_2O_5 and the refractive index were measured ellipsometrically ($\lambda = 632.8$ nm). Layers with thickness of 10 nm were studied. The refractive index is 2.1. The test structures were MOS capacitors with Al electrodes. Al electrodes were thermally evaporated by a conventional technique. The square capacitors with gate areas (*S*) of 2.5×10^{-3} cm^2 were defined by photolithography.

The high frequency *C-V* measurements were performed at 100 kHz with a HP 4284 A LCR meter, in the voltage range from –3 V through +1 V. The saturated capacitance value C_{ac} at accumulation was obtained by applying the extrapolation method used in [30]. This method provides an extrapolated value of saturated capacitance practically independent on the maximum gate voltage and hence on the variations of the flatband voltage. By using the standard methods [36], the values of the flatband voltage were subsequently determined.

The leakage currents were measured by using a HP 4140 A picoampermeter/DC voltage source, in the gate voltage (V_g) range from –3 V through +1 V. Current was measured in steps of 0.1 V, with a hold time of 5 s, enabling conditions of negligible displacement current.

RESULTS AND DISCUSSION

C-V characteristics

First, we studied *C-V* characteristics on fresh samples in the case where the first run consists of varying the gate voltage from +1 V to –3 V in steps of 0.1 V (run left). In the second run, performed 10 s after the end of the first one, the voltage is swept back from –3 V to +1 V (run right). The third run starts 10 s after the end of the second one from gate voltage of +1 V and goes to –3 V (Figure 1). Altogether, eight runs in alternate directions were performed. It is seen that the first run differs substantially from the third. The differences between the third run and the next runs left are much smaller, and hence they are not shown in Figure 1.

The same is valid for all the runs right. We can also speak about four consecutive sweeps composed of runs left followed by runs right. In order to give more precise description of the variations in the *C-V* characteristics, corresponding values of the flatband voltage for different sweeps for both the runs left (L) and the runs right (R) are given in Table 1. Values for d_{eq}, ΔV_{fb} for a given sweep and the corresponding variations in ΔQ_{ox} are also shown.
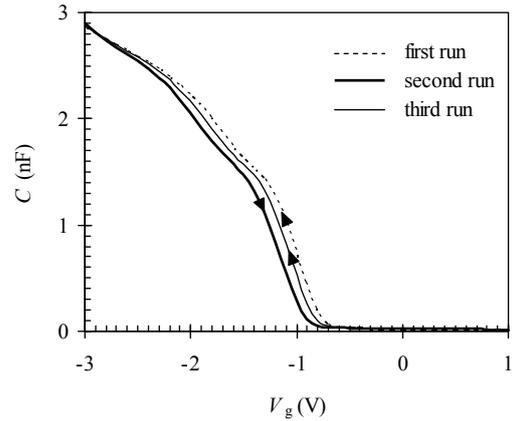

Figure 1. *C-V* characteristics obtained for three consecutive runs performed on fresh samples, first one starting from positive gate bias

Table 1. Flatband instability parameters for sweeps left–right

Sweep	$V_{fb,L}$ (V)	$d_{eq,L}$ (nm)	$V_{fb,R}$ (V)	$d_{eq,R}$ (nm)	ΔV_{fb} (V)	ΔQ_{ox} (cm^{-2})
First	−0.832	2.53	−1.006	2.45	0.174	15.7×10^{11}
Second	−0.911	2.46	−1.007	2.40	0.096	9.2×10^{11}
Third	−0.920	2.44	−1.010	2.39	0.090	8.6×10^{11}
Fourth	−0.925	2.44	−1.011	2.39	0.086	8.3×10^{11}

Significant decrease of ΔV_{fb} and ΔQ_{ox} is observed between the first and the second sweep. In addition, the equivalent oxide thickness decreases for about 0.06 nm. The decreases of d_{eq} after that appear to be not significant. It appears that saturation occurs after few sweeps at the values of ΔV_{fb}, ΔQ_{ox} and d_{eq} close to the values obtained in the second sweep. We made measurements for up to nine successive sweeps and observed that no further significant changes of *C-V* characteristics occur; since the differences for next sweeps are not significant, only the results for three to four first sweeps are shown here. The assumption that there is no further modification of the curves for next sweeps is valid in the limits of error of 5 mV for ΔV_{fb}, $5×10^{10}$ cm^{-2} for ΔQ_{ox} and 0.02 nm for d_{eq}. Since these errors are between the lowest for determination of the considered quantities, we may conclude that after the first sweep a repeatable hysteresis-like pattern is obtained when sweeping the voltage in a range without significant degradation (+1 V to –3 V for films as thin as 10 nm). Curves for further sweeps are not shown here since they can not be distinguished from the presented in the Figures 1 and 3. Additional feature to be noted is the difference between the values obtained for runs left and runs right of about 0.05 nm that do not fall in

the error limits. It is possible that the origin of this difference is the effect of slow states on the extrapolated value of capacitance in accumulation obtained by the method used in this work. Namely the method provides correction for leakage currents and fast interface states, but the slow interface states causing the hysteresis may produce some errors in the determined value of d_{eq}. Later we will discuss whether $d_{eq,L}$ or $d_{eq,R}$ is more influenced by the presence of slow interface states.

Initial degradation occurring during the first run left appears to be irreversible. In order to confirm this assumption, we repeated the above experiment, on a fresh capacitor, with a pause of 24 h between the first and the second sweep. No visible changes were observed compared to the case without long pauses.

Second, we measured the *C-V* characteristics on another capacitor for the case where in the first run the gate voltage varies from –3 V to +1 V and in the second run the voltage varies back from +1 V to –3 V (Figure 2). Repeatable hysteresis-like loops were obtained for three successive sweeps. The results for the second and the third sweep are not shown here, since there are no visible differences between the first and other hysteresis-like loops.
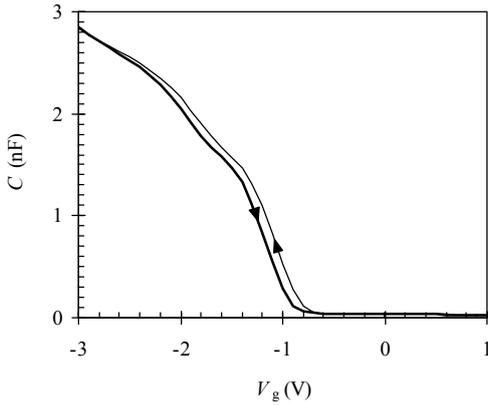
Figure 2. *C-V* hysteresis-like loop obtained when sweeping the gate voltage from –3 V to +1 V (right – R, thick line) then from +1 V to –3 V (left – L, thin line): only results for the first sweep are shown, the differences between the successive sweeps being very small

The corresponding values of the flatband voltage (V_{fb}) for different sweeps for both the runs right (R) and the runs left (L) are given in Table 2. As is seen from this table, the differences between the first and the second sweep are much smaller than in the case of sweeping first left then right. The situation is similar with the values for d_{eq}, ΔV_{fb} and ΔQ_{ox}. Variations in the values of d_{eq} of about 0.05 nm between these two capacitors appear. Measurements

performed on other capacitors give similar values with dispersion of around 3 %, most probably due to the thickness nonuniformity. Based on these observations, considering different sources of error, the error limit for the entire wafer can be set to about 0.1 nm. The error in ΔQ_{ox} would not exceed 1×10^{11} cm^{-2}. Therefore, the measured value for the first sweep left then right is 1.57×10^{12} cm^{-2} (Table 1) and for all other values given in Tables 1 and 2, $(8.6 \pm 0.6) \times 10^{11}$ cm^{-2}. The second value $((8.6 \pm 0.6) \times 10^{11}$ cm$^{-2})$ is connected to a repeatable feature of the flatband voltage instability for the considered structure. This instability in principle can be related either to the trapping on slow traps or to the charging of the interface between the Ta_2O_5 and the interfacial SiO_2 layer. Since the charging of the considered interface would result in a clockwise loop [23], we conclude that the dominant effect is that of charging slow states by injection of carriers from the substrate. Mobile charge and polarization effects are also excluded since they would result in a clockwise loop, as well as the injection from the gate. The first value $(1.57 \times 10^{12}$ cm$^{-2})$ is substantially larger and involves in addition an initial ireversible effect. Further, we shall discuss in more details only the repeatable effect of charging/discharging leading to the flatband voltage instability.

Table 2. Flatband instability parameters for sweeps right–left (second capacitor)

Sweep	$V_{fb,R}$ (V)	$d_{eq,R}$ (nm)	$V_{fb,L}$ (V)	$d_{eq,L}$ (nm)	$\Delta V_{fb,R}$ (V)	ΔQ_{ox} (cm^{-2})
First	–0.910	2.52	–1.003	2.50	0.093	8.1×10^{11}
Second	–0.922	2.49	–1.012	2.44	0.090	8.4×10^{11}
Third	–0.930	2.48	–1.015	2.44	0.085	8.0×10^{11}

Next, we measured the *C-V* characteristics on a separate capacitor while in the first run the gate voltage varies from V_L to +1 V and in the second run the voltage varies back from +1 V to V_L, for values of V_L ranging from –3 V to –1 V (Figure 3). Repeatable hysteresis-like loops obtained for narower ranges are tighter than the loops for wider ranges. Variations of the ΔV_{fb} versus V_L are shown in Figure 4. It is seen that ΔV_{fb} increases linearly with the absolute value of the gate voltage. The onset appears at a value of about 0.9 V, close to $V_{fb,R}$. In the case of such thin films, it is impossible to obtain saturation without degradation. As we found on structures containing 50 nm thick Ta_2O_5 layers, saturation occurs at voltages 4 V to 5 V. At such high gate voltages significant wearout and even destructive breakdown occurs. In order to estimate the saturation

value, we made a simple linear extrapolation of the ΔV_{fb} value up to 4 V giving $\Delta V_{fb} = 0.12$ V, that corresponds to a charge density of 1.28×10^{12} cm^{-2}.

In order to describe in more details the charging process, i.e. to determine whether the trapping on slow states of electrons or holes injected from the substrate determines the instability feature, we determined the points where the variation of the capacitance changes the direction (return points). In Figure 5 an illustration for the return points for different maximum negative voltages for sweeps right–left is given. It is seen that the return points are located on a curve close to the curves obtained for the runs left. Thus, it can be concluded that for the sweeps right–left, the runs left follow approximately a unique curve and only the runs right differ between them.
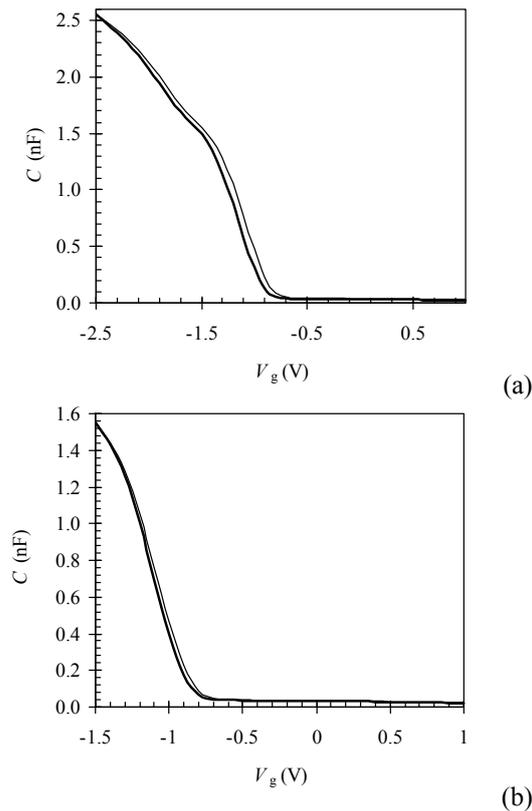
(a)

(b)

Figure 3. Hysteresis-like loops obtained when sweeping the applied voltage from a given value V_L to +1 V (right – R, thick line) then from +1 V to V_L V (left – L, thin line) for two different V_L values: $V_L = -2.5$ V (a) and $V_L = -1.5$ V (b)
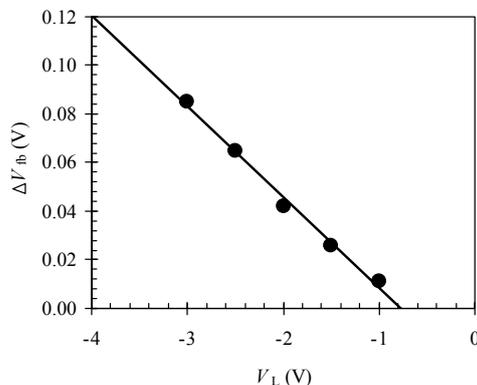

Figure 4. Flatband voltage difference between the runs right (from V_L to +1 V) and left (from +1 V to V_L) versus V_L; an almost linear increase with the absolute value of the voltage is observed with onset at about –0.9 V

The above finding can be explained as follows. At negative voltages holes are injected from the silicon substrate [25]. Part of them is captured by slow traps in the interfacial silicon oxide layer. The density of the captured holes and hence the positive charge on slow states increases with the increasing absolute value of the negative

voltage during the runs left, until maximum or saturated value. During the runs right at negative voltages the density of trapped positive charges remains as obtained at the maximum negative voltage. At highest positive voltages at the end of the run right, electrons are injected from the substrate [25] thus neutralizing the positive charge previously captured on slow states. Contrary to the case of thicker films studied in [23], in our case no effects of the hold time up to 100 s at the return points were observed. Based on all above presented findings we can conclude that the observed loops are due to the trapping of holes on slow interfacial traps, rather than to the charging of the interface between the Ta$_2$O$_5$ bulk and the SiO$_2$ interfacial layer. Thus, saturated value of the ΔQ_{ox} can be regarded as slow states density Q_{sl}. For our samples the estimated value obtained by extrapolation is $Q_{sl} = 1.3 \times 10^{12}$ cm^{-2}. For very thin films the values of Q_{sl} obtained directly from hysteresis-like loops appear to be underestimated, since the voltage range for measurement without significant degradation is limited to values as low as 3 V or lower.
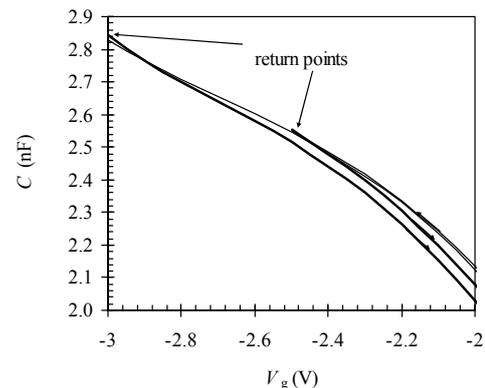

Figure 5. Return points for different maximum negative voltages for sweeps right-left; return points are located on a curve close to the curves obtained for the runs left

J-V characteristics

Similarly to the case of *C-V* measurements, *J-V* measurements for different sweeping directions were done. First we show *J-V* characteristics of the structures on fresh samples when the first run consists of varying the gate voltage from +1 V to –3 V in steps of 0.1 V. In the second run, performed 10 s after the end of the first one, the voltage is swept back from –3 V to +1 V (Figure 6). As is seen in this figure, the curves for these two runs are substantially different. Nevertheless, while performing following runs, these differences practically disappear, contrary

to the case of *C-V* characteristics. The only exception is that of very low gate voltages (–0.1 V) where the current density for the run left is substantially lower than that for the run right.
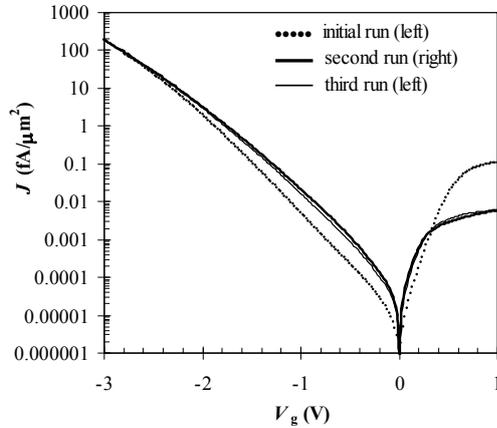

Figure 6. *J-V* characteristics for first three consecutive runs: first run from +1 V to –3 V (dots), second run from –3 V to +1 V (thick line) and third run from +1 V to –3 V (thin line)

Next we made the *J-V* measurements where the first run on fresh samples is done while varying the gate voltage from –3 V to +1 V in steps of 0.1 V. In the second run, performed 10 s after the end of the first one, the voltage is swept back from +1 V to –3 V. In this case, the curves for the two runs do not differ as in the case shown in Figure 6. Similarly, while performing next runs, no significant differences are observed. Again, the only exception is that of very low gate voltages (–0.1 V) where the current density for the run left is substantially lower than that for the run right. The graphs for these results are not shown here, since the three consecutive first sweeps give practically the same results as those shown in Figure 6. We disregard the saturation part of the curve in inversion (maximum positive voltages) since the current there is limited by the substrate minority carrier density, which is not of interest for this study.

Leakage current analysis based on the comprehensive model for metal-Ta_2O_5/ SiO_2-Si capacitors [28] gives observable changes in the interfacial layer thickness, d_{it}. For the first run left performed on fresh samples we obtain the value d_{it} = 1.85 nm. For the returning run right, as well for other subsequent runs, the thickness value is slightly lower (d_{it} = 1.77 nm). When starting with the run right, the thickness value of 1.77 nm is obtained for all the runs. The above finding is in

accordance with the variations of the equivalent oxide thickness extracted from *C-V* measurements, where the highest value of 2.53 nm was obtained for the first run right on fresh samples. The observed decrease of the equivalent dielectric thickness of the Ta_2O_5/SiO_2 stack can be attributed to the decrease of the effective physical thickness of the interfacial SiO_2 layer by creation of percolation paths in a part of the interfacial region [37]. This finding is in accordance with the results we obtained in [28], where at higher fields the decrease of the interfacial layer thickness progresses very rapidly in the first stage of few seconds.

Other related issues

Both for the *C-V* and the *J-V* characteristics it is observed that the first run left (from +1 V to –3 V) gives essentially different results from all other runs, i.e. the measurements do not only sample the existing traps (or charges) but generate new ones. This can be explained by the degradation that occurred at maximum negative voltages applied at the end of the run (–3 V). At this voltage a leakage current density of about 20 mA/cm^2 is obtained due to the injection of holes from the substrate [25]. Even if the measurement time is short (of order of 10 s), partial consumption of the interfacial layer occurs by creation of conductive paths in it (most probably composed of newly generated traps), leading to a small decrease in the effective thickness of this layer of about 0.1 nm [27]. This process seems to progress rapidly at the beginning and much slower for longer stresses, as it was observed in [27]. As a result of this, equivalent oxide thickness decreases also for about 0.1 nm. While performing next runs, interfacial layer thickness is much less affected. When starting with a run right, the same degradation as above occurs during the initial stage of the measurement (at –3 V), and hence much less significant differences are obtained between the first and the third run.

For the case of *C-V* characteristics the first run gives flatband voltage (–0.832 V) much lower than the following run left (about –0.92 V). This irreversible change could not be accounted for by the change in the interfacial layer thickness. Most probably during the first run left some slow state charges are compensated by electrons injected from the gate into the tantalum pentoxide layer. Again, when starting at highest negative voltages, this degradation occurs at the beginning of the measurement, and hence does not produce differences between the different runs.

It is seen that the determined equivalent oxide thickness values are different for runs left and right, although the maximum capacitances are practically the same. The above is due to the fact that we determine the thickness by an extrapolation method and hence the extrapolated saturated values differ because of the differences in the other parts of the curves. The correct curve to be used in determination of the equivalent oxide thickness is the curve for the run right, since there is no detrapping of the charges on slow traps during the part of the run in accumulation, which is the part used in the extrapolation method. Similarly, the determination of the fast interface state densities has to be done while using the curves obtained at runs right.
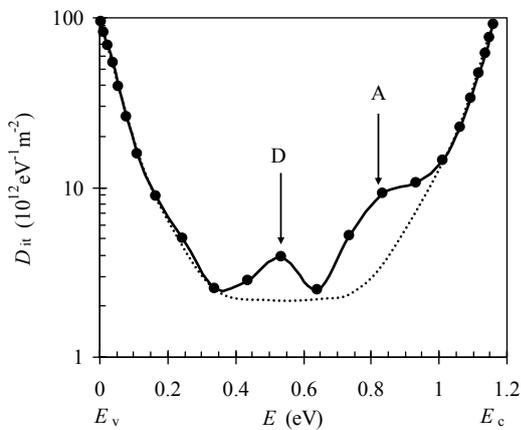

Figure 7. Fast interface state density distribution determined from the *C-V* curves obtained at a run right

The result for the distribution of fast interface state densities (D_{it}) over the forbidden band, obtained by a standard Terman method [36] from the high-frequency *C-V* characteristic, is given in Figure 7. Zero energy (E) level corresponds to the top of the valence band. The tails of the U-D_{it} curve close to the forbidden band edges can be explained by the "U-shaped" continuum of band edge states typical of Si/SiO$_2$ interfaces [31]. Usually observed flat part close to the midgap was not found (broken line). Instead of that, there are two relatively well defined peaks. The peak at 0.53 eV corresponds to a trap level located in Ta$_2$O$_5$ dielectric 0.68 eV below the conduction band edge. Practically the same value (0.7 eV) was found in [32] for the electron trapping centres responsible for the leakage currents in Ta$_2$O$_5$. This value is close to the value of the activation energy of the traps of type D (0.8 eV), found in [33] using zero-bias thermally stimulated current spectroscopy and attributed to the first ionization level of the double-donor

oxygen vacancy and later theoretically explained in [34]. The second much broader peak is located at approximately 0.9 eV from the valence band of silicon, which corresponds to approximately 0.3 eV from the conduction band of Ta$_2$O$_5$. It corresponds to the trap that has been attributed to the Si/O-vacancy complex shallow single donor (type A, 0.2 to 0.4 eV) [35]. Doted line corresponds to an idealized U-shaped distribution without peaks, with a flat part in the middle of the bandgap at about 2.2×10^{12} eV^{-2}cm^{-2}.

In regard to *J-V* characteristics, one would expect to observe similar hysteretic behaviour as in *C-V* characteristics. Namely, if the sole reason for modification of *J-V* characteristics was the variation of V_{fb} due to trapping of charges on slow states as in the case of *C-V* characteristics, according to (1) the *J-V* curve for runs left had to be simply shifted for the value ΔV_{fb} on the voltage axis. Indeed, the positive charge in the interfacial layer affects similarly the leakage currents as it affects the capacitances. This effect is explained further. For negative oxide voltages, injection of holes from silicon substrate occurs [26, 38]. During the run left at highest negative voltages trapping of holes in the interfacial layer occurs, as manifested by the V_{fb} shift. During the run right, negative oxide voltage decreases and the trapped charge remains unaffected. Leakage current is a function of the voltage drop on the stacked insulating layer (V_{ox}). This voltage is determined by using relation involving the flatband voltage (V_{fb}) and the voltage drop in the semiconductor (V_s) [39]:

$$V_{ox} = V_g - V_{fb} - V_s \qquad (1)$$

Flatband voltage for the runs left is negative and its absolute value is lower than for the runs right, due to the positive trapped charge on slow states. As a result, voltage drop on the insulating layer is bigger for the runs right than for the runs left, for the same applied gate voltage. Therefore, if there are no other differences, it is expected the leakage current to be higher for the runs right than for the runs left. On the other hand, the positive trapped charge in the interfacial layer (Figure 8) modifies the barrier for Fowler-Nordheim and direct tunneling injection of holes. Due to these charges, a modified barrier with lower trans-missivity than in the case of absence of charges in the interfacial silicon oxide layer is obtained. Thus, a second effect leading to a decrease of the leakage current with the presence of positive trapped charge on slow states in the interfacial layer is present. These two effects modify the leakage current in

opposite directions. Due to mutual compensation of these two contributions, the *J-V* characteristics for the runs left and the runs right look quite similar. Nevertheless, there are visible differences for gate voltages close to zero. For these voltage values the leakage currents for the runs right are higher than for the runs left. However, these currents are very low and it is possible to be due to some transient effects. Nonetheless, these differences are very small (less than $0.1 \, fA/\mu m^2$) and can be neglected for practical purposes.
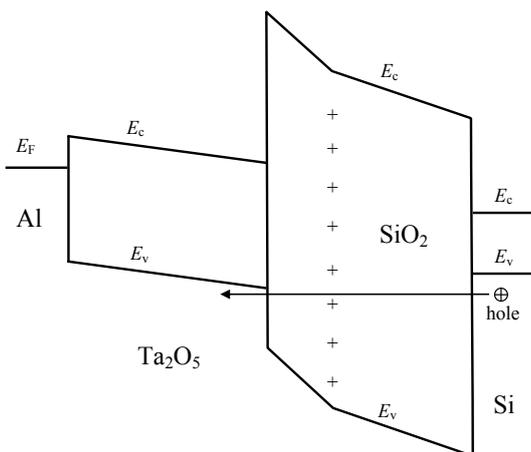

Figure 8. Modification of tunnelling barrier due to the presence of trapped positive charge in the interfacial layer

Therefore, the static *J-V* characteristics except for the initial run left do not exhibit hysteretic behaviour. Observed instabilities when measuring *J-V* characteristics with rapidly changing voltages are due to the displacements and transient currents.

It is important to emphasize the essential difference between the results obtained for thicker films in [22, 23] and here obtained results on films as thick as 10 nm. In both cases samples present Al-Ta_2O_5/SiO_2-Si structures. The composition of the interfacial layer in both cases is practically the same; it is an SiO_2-like layer. The dominant hysteretic pattern in [23] is the clockwise hysteresis, while in this work counterclockwise hysteresis is observed. The above is due to different charging mechanisms. In the case of thicker films the interface Ta_2O_5/SiO_2 at highest negative voltages is charged with electrons flowing from the metal gate through the leaky Ta_2O_5 dielectric. In the range of applied voltages (–3 V to +1 V) the SiO_2-like interfacial layer is non-conductive. As a result, negative charge accumulates at the Ta_2O_5/SiO_2 interface. In our case, tunnelling of holes from the substrate at negative voltages occurs. Electrons can not accu-

mulate at the Ta_2O_5/SiO_2 interface since there is a flow of holes and recombination occurs instead of accumulation. Only the positive charge trapped on slow states in the interfacial layer contributes to the hysteretic behaviour. These traps being located between two interfaces (Ta_2O_5/SiO_2 and SiO_2-Si) and energetically enough deep, retain the positive charge trapped at highest negative voltages until reaching certain value of the positive voltage (of about 1 V). The electrons injected by Fowler-Nordheim mechanism from the substrate neutralize the positive trapped charge in the interfacial layer. As a result, counterclockwise hysteresis is obtained.

CONCLUSIONS

Except for the first run left performed on fresh samples, when sweeping the voltage in a range without significant degradation (+1 V to –3 V for films as thin as 10 nm), the *C-V* and *J-V* characteristic exhibit repeatable patterns. Small initial consumption of the interfacial layer occurs during this first run, leading to irreversible changes. Repeatable counter clockwise hysteresis-like loop is present in *C-V* characteristics. There is no significant hysteretic behaviour in static *J-V* characteristics. Although there are some differences in leakage currents between runs left and right for the voltages between zero and the flatband voltage, they are small and in accumulation they are definitely negligible. The hysteresis-like loop in the *C-V* characteristics can be entirely attributed to the trapping of holes on slow traps in the interfacial layer. Hysteretic behaviour is not observed in *J-V* characteristics since the effect of positive charge trapping on slow states is compensated by the effect of modification of the barrier for Fowler-Nordheim tunnelling of holes from the Si substrate.

Contrary to the case of thicker films studied in [23], in our case no effects of the hold time up to 100 s at the return points between the runs right and left for *C-V* characteristics were observed. The findings here show that the general results obtained on thicker films can not be applicable on thinner films, as studied here. The main reason for this is the low value of the thickness of the interfacial SiO_2-like layer (2 nm or less), in which case carrier transport through this layer occurs also at low voltages used in *C-V* measurements. Owing to the Fowler-Nordheim, direct and trap-assisted tunnelling as well as hopping, the charge accumulation at the interface between the high-*k* Ta_2O_5 layer and the interfacial SiO_2-like layer is substantially reduced.

Since trapping on slow states occurs when increasing the absolute value of the negative gate

voltage, *C-V* curves obtained during the runs left are distorted and hence they are not convenient for determination of the equivalent oxide thickness and fast interface state densities. It is better to use the curves obtained during the runs right, since there is no trapping or detrapping at negative voltages. Nevertheless, the parts of the curves obtained during the runs left up to the flatband voltage can be used, since there is no trapping on slow states until this value. Oxide charge is to be determined using the value of the flatband voltage obtained from the curve for the run left (after a run right), since it corresponds to the state of empty slow traps. The value obtained from the run right is equal to the sum of the fixed oxide charge and the charge trapped on slow states.

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НЕСТАБИЛНОСТИ СЛИЧНИ НА ХИСТЕРЕЗИС КАЈ НАПОНОТ НА РАМНИ ЗОНИ ВО СТРУКТУРИ Al/Ta$_2$O$_5$-SiO$_2$/Si И НИВНАТА ПОВРЗАНОСТ СО *J-V* КАРАКТЕРИСТИКИТЕ

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Нестабилностите во напонот на рамни зони и струјно-напонските карактеристики на структурите Al/Ta$_2$O$_5$-SiO$_2$/Si се проучени во детали. Најдено е дека, по едно почетно поминување налево на свежи обрасци, и *C-V* и *J-V* карактеристиките пројавуваат повторливи мостри. Кај *C-V* карактеристиките се јавува прецизно повторлива петелка слична на хистерезис, кај *J-V* карактеристиките не се набљудува забележливо хистерезисно поведение. Намалената нестабилност кај *J-V* карактеристиките е објаснета со меѓусебна компензација на два спротивни ефекта коишто се должат на зафаќањето на позитивни полнежи на бавни стапици во меѓуповршинскиот слој сличен на SiO$_2$: (i) поместувањето на напонот на рамни зони и (ii) намалувањето на бариерите за тунелирање од типот на Фаулер-Нордхајм за шуплините што се инјектираат од подлогата. Коректното определување на еквивалентната дебелина на оксидниот слој и густините на брзите меѓуповршински состојби бара употреба на *C-V* криви добиени при поминување надесно, затоа што при поминувањата налево се јавува прогресивно зафаќање на бавни состојби. Вредноста на полнежот во оксидот треба да се определи од вредностите на напонот на рамни зони добиени од поминувањата налево (по почетно поминување надесно), затоа што тоа одговара на состојбата на празни бавни состојби.

Клучни зборови: хистерезис на *C-V* карактеристиките; нанодимензионални диелектрични филмови; меѓуповршина силициум/силициум диоксид